Ku-Band 20 W Power GaAs FETs

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ABSTRACT

High power Ku-band internally matched GaAs FETs have been developed using multi-chip power combiner/divider technology. An output power of 43.2 dBm at 1 dB gain compression with 6.9 dB gain and 29.5 % power-added-efficiency has been obtained at 14 GHz. This state-of-the-art performance has been achieved by (1) optimizing the carrier concentration profiles of the active layer and making the buffer layer resistivity higher, (2) adopting the double-recess structure to get the higher breakdown voltage and (3) designing the high efficiency power combiner/divider circuits.

1. Introduction

High power GaAs FETs are the key devices for solid-state-power-amplifiers (SSPAs) operable at frequencies higher than C-band. Higher output power and power-added-efficiency (PAE) have been continuously pursued for radar and communication applications. Althought an output power of 30 W was reported at C-band [1], it is still limited to around 10 W at Ku-band [2],[3]. This limited power seems to be due to the difficulties in power combinig of the chips and in obtaining the enough power density and gain at Ku-band.

In this paper, we report on the performances of the newly developed Ku-band internally-matched GaAs MESFETs. An output power of 43.2 dBm (20.9 W) at 1 dB gain compression with 6.9 dB gain and 29.5 % PAE at 14 GHz has been obtained by using multi-chip power combiner/divider technologies and increasing the output power density of the single FET chip.

2. Design and fabrication process of the FET chip

In order to increase power density of the single FET chip, it is important to make the maximum channel current and drain breakdown voltage higher. In this study, carrier concentration of the active layer is increased up to 4.5 x 10^{17} cm^{-3} to enhance the maximum channel current. A high resistive AlGaAs buffer layer is introduced to get a clear pinch-off and improve a drain conductance. Moreover, a double-recess structure is adopted to increase the drain breakdown voltage.

A cross-sectional view of the fabricated GaAs MESFET chip is schematically shown in Fig. 1. The epitaxial wafer consists of a 100 nm-thick undoped $Al_{0.2}Ga_{0.8}As$ layer, a 200 nm-thick undoped GaAs layer, a 110 nm-thick n-GaAs channel layer, a 100 nm-thick n^--GaAs layer and a 100 nm-thick n^+-GaAs cap layer, successively grown by MOCVD on a

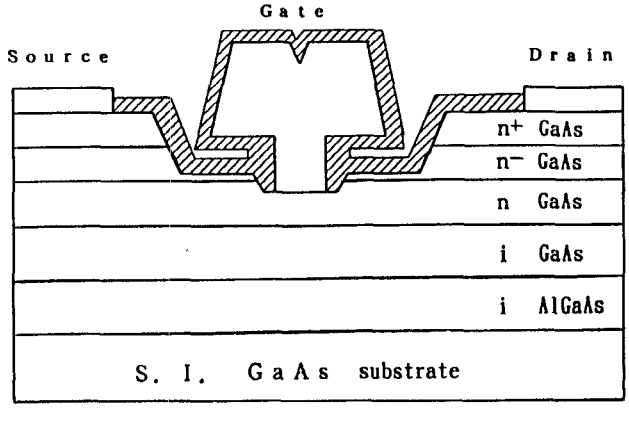

Fig.1 Shematic cross section of fabricated GaAs MESFET. (gate length; 0.5μm, gate finger width; 96μm)

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Cr-doped semi-insulating GaAs substrate. Insertion of an undoped $Al_{0.2}Ga_{0.8}As$ layer has been found to be effective to increase the resistivity of the buffer layer, thereby giving the clear pinch-off and small drain conductance to improve the power gain of the FETs. Carrier concentrations of the n^+-GaAs cap layer, n^--GaAs layer and n-GaAs channel layer are 2 x 10^{18} cm^{-3}, 5 x 10^{16} cm^{-3}, 4.5 x 10^{17} cm^{-3}, respectively, doped with Si. High carrier concentration of the channel layer is indispensable to obtain high transconductance and maximum channel current.

An active area is defined by mesa etching, and the source and drain electrodes are formed by alloying of Ni/AuGe. The source-drain spacing is 8 μm. The double-recess strucure, with wider and narrower spacings of 1.5 μm and 0.6 μm, respectively, is adopted to increase the drain breakdown voltage. The gate has T-shaped cross section with Ti/Al to reduce the gate resistance. The gate length and unit gate finger width are 0.5 μm at the foot print and 96 μm, respectively. Silicon nitride with thickness of 200 nm is used as a passivation film.

Fig. 2 shows a top view of the fabricated GaAs FET chip. The total gate width is 19.2 mm with 200 gate fingers. The chip size is 3.4 mm × 0.6 mm. Air bridges and via holes are formed to reduce the parasitic capacitance and inductance. To improve thermal resistance, the GaAs substrate is thinned to 40 μm and a gold PHS (plated-heat-sink) with 50 μm thickness is formed on the backside of the substrate.

3. DC characteristics

DC characteristics are measured for the TEG (Test Elemental Group) FETs (2 fingers, Wg=192μm), which is fabricated on the same wafer. Figs. 3 and 4 show the results, where the gate voltage is applied from 1 V to −4 V. The drain saturation current (Idss) is around 55 mA (290 mA/mm) and the maximum drain current (Idsmax) is around 85 mA (440 mA/mm). The ratio of Idsmax/Idss of the developed FET is around 1.5, which seems to be high enough for obtaining high output power density. The clear pinch-off and the small drain conductance is

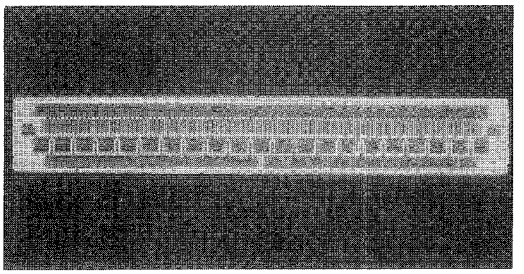

Fig.2 The top view of the FET chip.
(Wg; 19.2 mm, chip size; 3.4mm × 0.6mm)

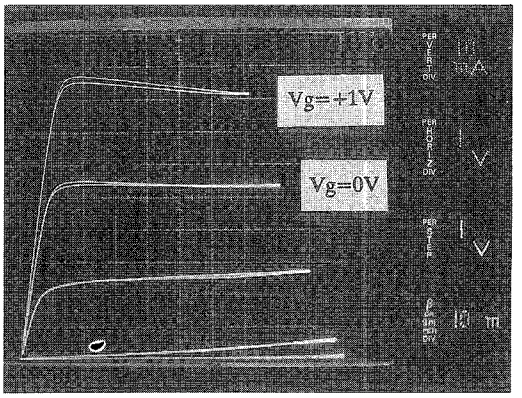

Fig.3 DC characterisitics of TEG FET (Wg=192 μm).

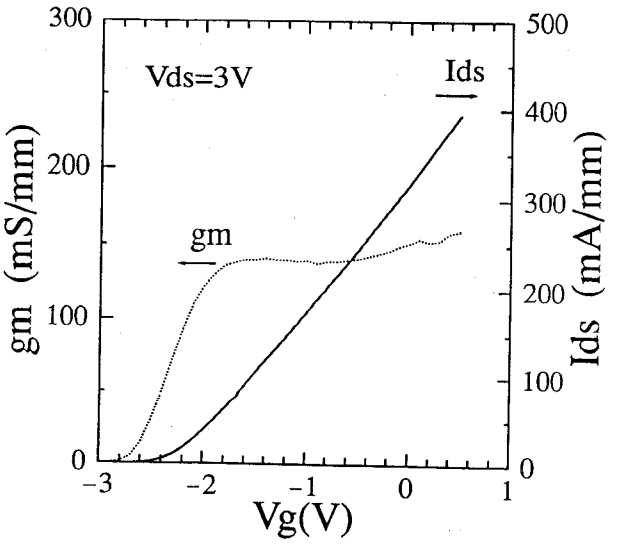

Fig.4 Vg dependence of gm and Ids for TEG FET (Wg=192 μm).

obtained as shown in Fig. 3. The maximum transconductance (gm) of the FET is around 30 mS (160 mS/mm), which is relatively high as compared with the reported MESFETs [2] operating at Ku-band.

The three-terminal drain breakdown voltage is around 13 V, when defined at a drain current of 1 mA/mm.

4. RF performance of single FET chip

Fig. 5 shows the power performance of the single FET chip (Wg=19.2 mm) measured at 14 GHz. The FET is assembled in the package with internal matching circuits. It is biased at Vds=9 V and Ids= 1/2 Idss. An output power of 40.4 dBm at 1 dB gain compression (P1dB) with 7.0 dB gain has been obtained. The obtained power density has been 570 mW/mm, which is almost the same as the highest one of the reported GaAs MESFETs operating at Ku-band.

5. Design of the matching circuits

Matching circuits are designed to combine the output powers of the FET chips.

Fig. 6 shows the equivalent circuit of the developed power combiner/devider. Both the input and output internal matching circuits are 2-section LC low pass filter network, where the bonding wires and chip capacitors are used as an inductor and capacitors, respectively. Fig. 7 shows the inner view of the assembled FET, consisting of two FET chips, two chip capacitors and input/output distributed matching circuits. A ceramic subatrate with low relative dielectric constant (ε r=5) is used for the output distributed circuits to get a good power combining efficiency. For input distributed circuits, the conventional alumina substrate (ε r=9.5) is used The package size is 21mm x 12.9mm. It is to be noted that this package size is as small as that of Toshiba's commercially available Ku-band 8W/10W internally matched power FETs [4].

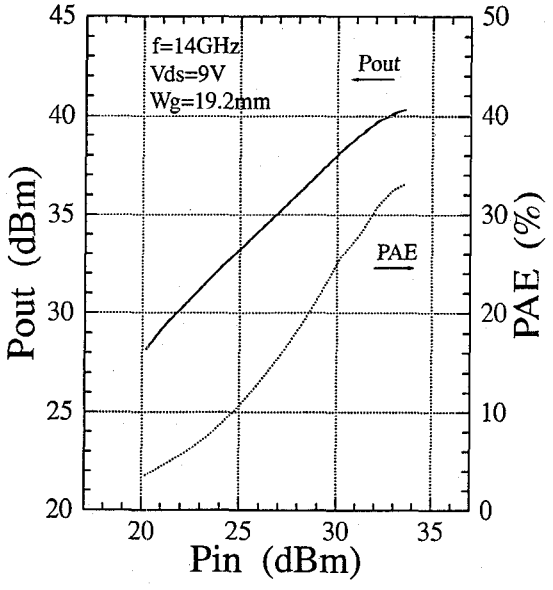

Fig.5 Output power and PAE versus input power of the single FET chip.

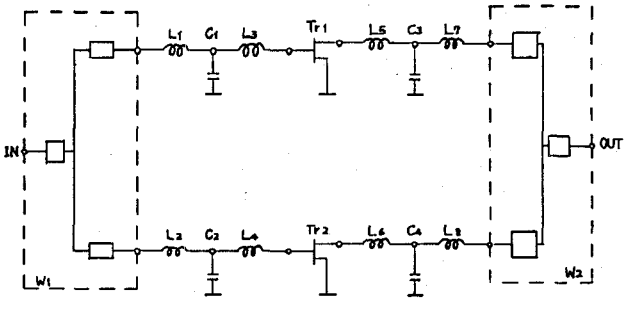

Fig.6 The equivalent circuit.

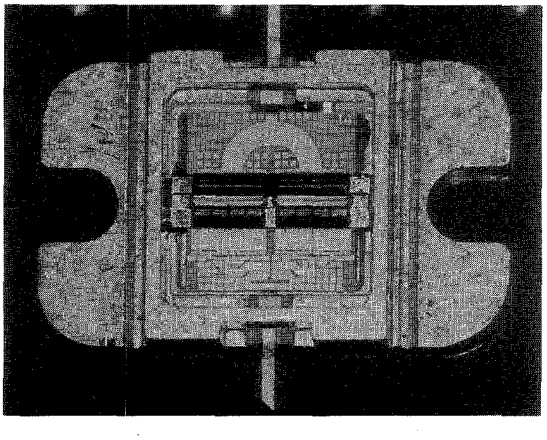

Fig.7 Inner view of the Ku-band internally matched GaAs FET. (package size; 21mm x 12.9mm)

6. RF performance

Fig. 8 shows an output power and PAE versus input power characteristics at 14 GHz for the developed internally matched FET. An output power of 43.2 dBm (20.9 W) at P1dB with 6.9 dB gain and 29.5 % PAE has been obtained at the biasing point of Vds=9 V and Ids = 1/2 Idss. The power combinig efficiency has been estimated to be about 95%. A saturated output power has been 43.4 dBm (21.9 W) with a PAE of 29.2 %. This is the highest output power reported so far of GaAs FETs at Ku-band.

7. Conclusion

High power Ku-band internally matched GaAs FETs have been developed using multi-chip power combiner/divider technologies. State-of-the-art performances of an output power of 43.2 dBm with 6.9 dB gain and 29.5 % PAE has been obtained at 14 GHz. The developed FETs will be applicable to the variety of SSPAs used in rader and communication systems which require higher output power.

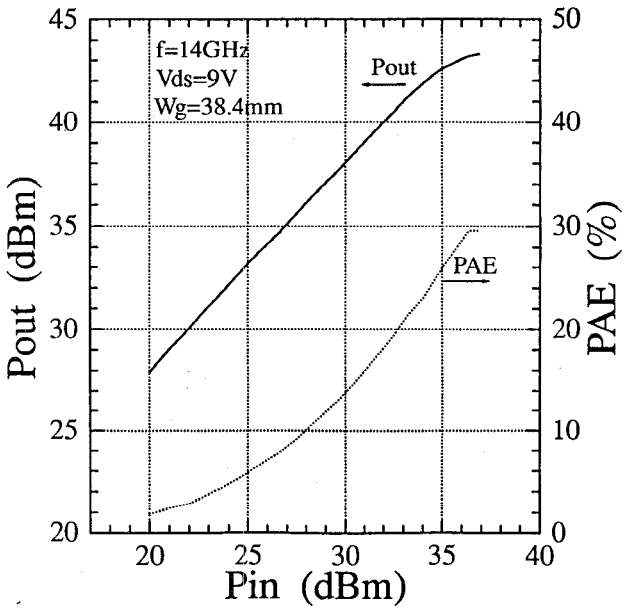

Fig.8 Output power and PAE versus input power of the GaAs FETs measured at 14GHz.

Acknowledgment

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